Listing of Claims:

1. (previously amended) A method for increasing yield of usable memory locations in an embedded memory device, the method comprising:

providing a cache for a memory unit;

determining when an access is made to a failed bit memory location in the memory unit, wherein determining when an access is made further comprises identifying each failed bit location in the memory unit and storing each failed bit location in the cache, wherein storing further comprises storing each failed bit location in a look-up table; and

substituting a memory location in the cache for the failed bit memory location when the failed memory bit location is accessed.

2. Previously Canceled.

3. Previously Canceled.

4. (previously amended) The method of claim 1 wherein determining further comprises comparing a memory location being accessed to identified failed bit locations.

5. (previously amended) The method of claim 1 wherein identifying each failed bit location further comprises performing a pre-scan operation on the memory unit.

6. (original) The method of claim 1 wherein providing a cache further comprises providing an SRAM.

7. (original) The method of claim 1 wherein the memory unit further comprises a DRAM unit.

8. (previously amended) A method for increasing yield of usable memory locations in an embedded memory device, the method comprising:

performing a memory pre-scan operation on an embedded memory device to identify each failed bit location in the embedded memory device;

storing each failed bit location in a look-up table; and

swapping a memory location within a cache for a failed bit location.

9. (original) The method of claim 8 further comprising providing the cache between a memory unit and a memory control unit in the embedded memory device.

10. (original) The method of claim 8 further comprising storing each failed bit location in a look-up table in the cache.

11. (original) The method of claim 8 wherein swapping a memory location further comprises swapping when an access attempt is made to a failed bit location.

12. (original) The method of claim 11 further comprising swapping by a memory control unit for the embedded memory device.

13. (original) The method of claim 8 wherein the memory unit further comprises a DRAM unit.

14. (original) The method of claim 8 wherein the cache further comprises an SRAM unit.

15. (previously amended) An embedded memory device with increased yield of usable memory locations, the embedded memory device comprising:

a memory unit;

a cache coupled to the memory unit; and

a memory control unit coupled to the memory unit and the cache, the memory control unit determining when an access is made to a failed bit memory location in the memory unit, and substituting a memory location in the cache for the failed bit memory location when the failed memory bit location is accessed, wherein determining when an access is made further comprises identifying each failed bit location in the memory unit and storing each failed bit location in the cache, wherein storing further comprises storing each failed bit location in a look-up table.

16. (original) The embedded memory device of claim 15 wherein the memory unit further comprises a DRAM.

17. (original) The embedded memory device of claim 15 wherein the cache further comprises an SRAM.

18. (original) The embedded memory device of claim 15 wherein the memory control unit further identifies each failed bit location in the memory unit and stores each failed bit location in the cache.

19. (original) The embedded memory device of claim 18 wherein the memory control unit further compares a memory location being accessed to the identified failed bit locations.

20. (original) The embedded memory device of claim 15 further comprising an embedded memory module of a graphics accelerator.